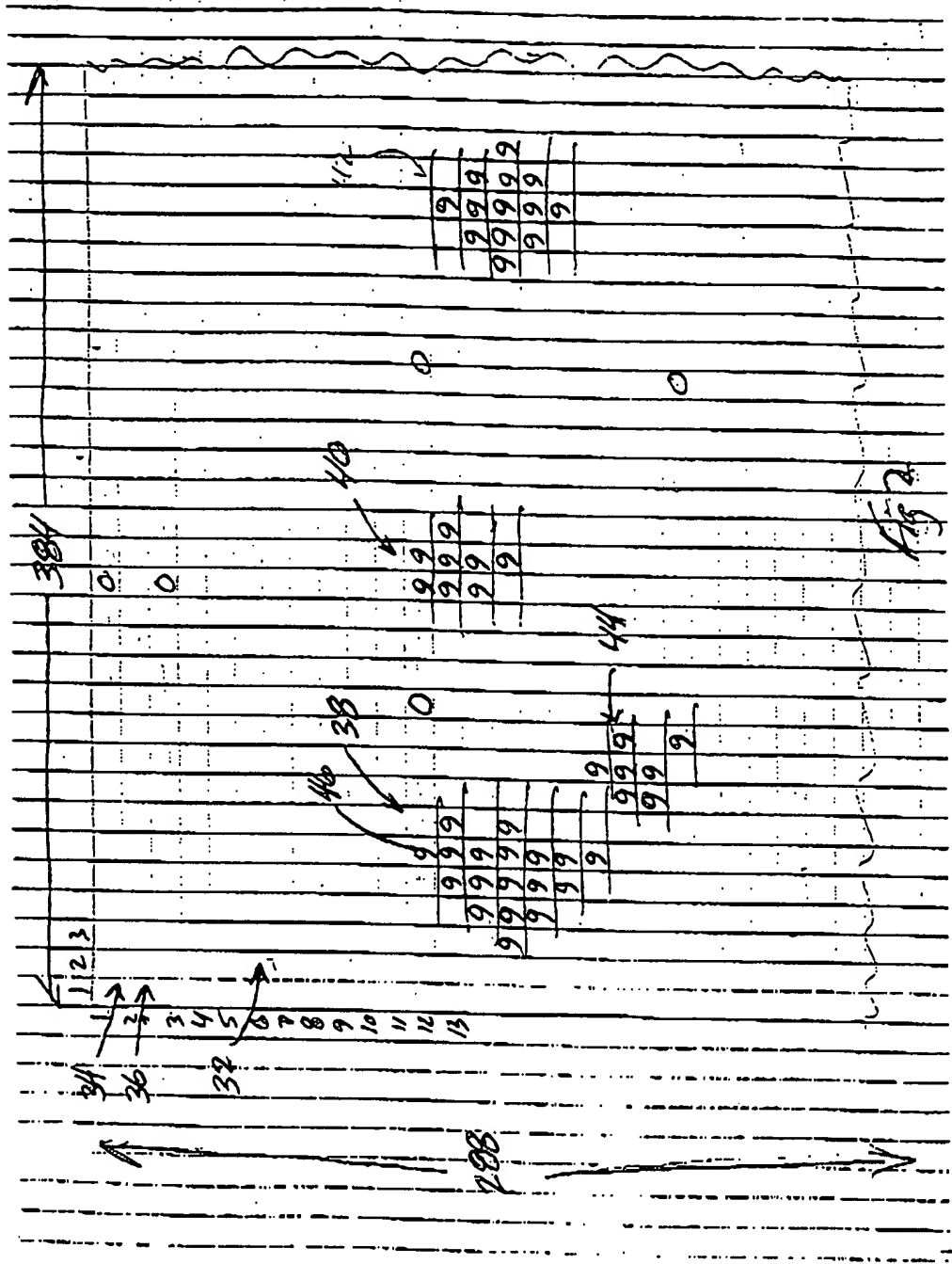


FIG. 1

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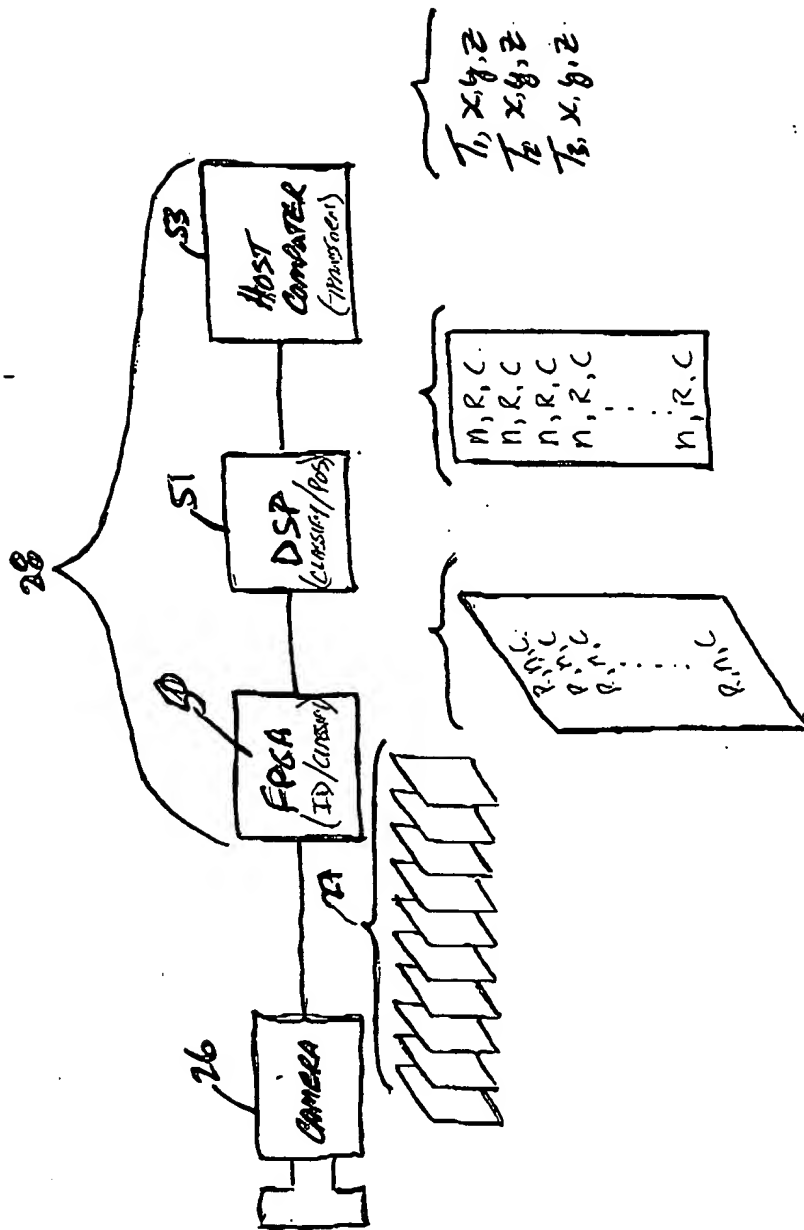
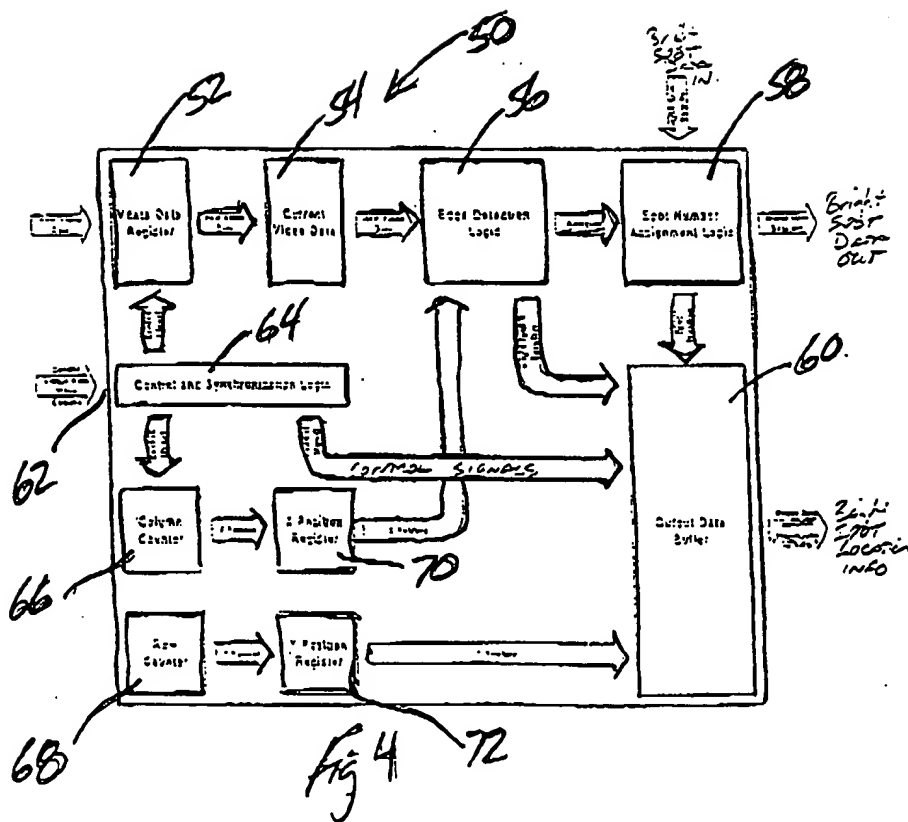
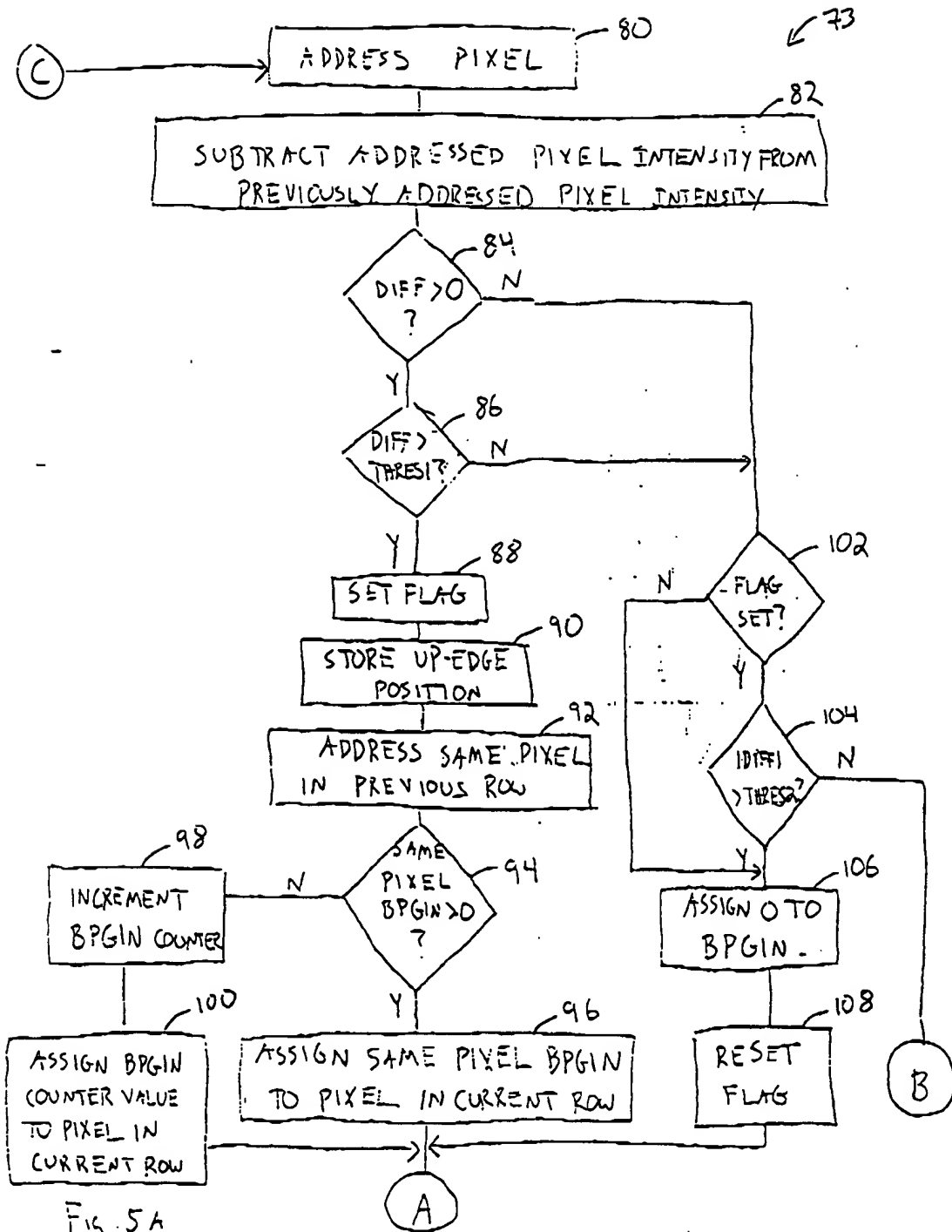
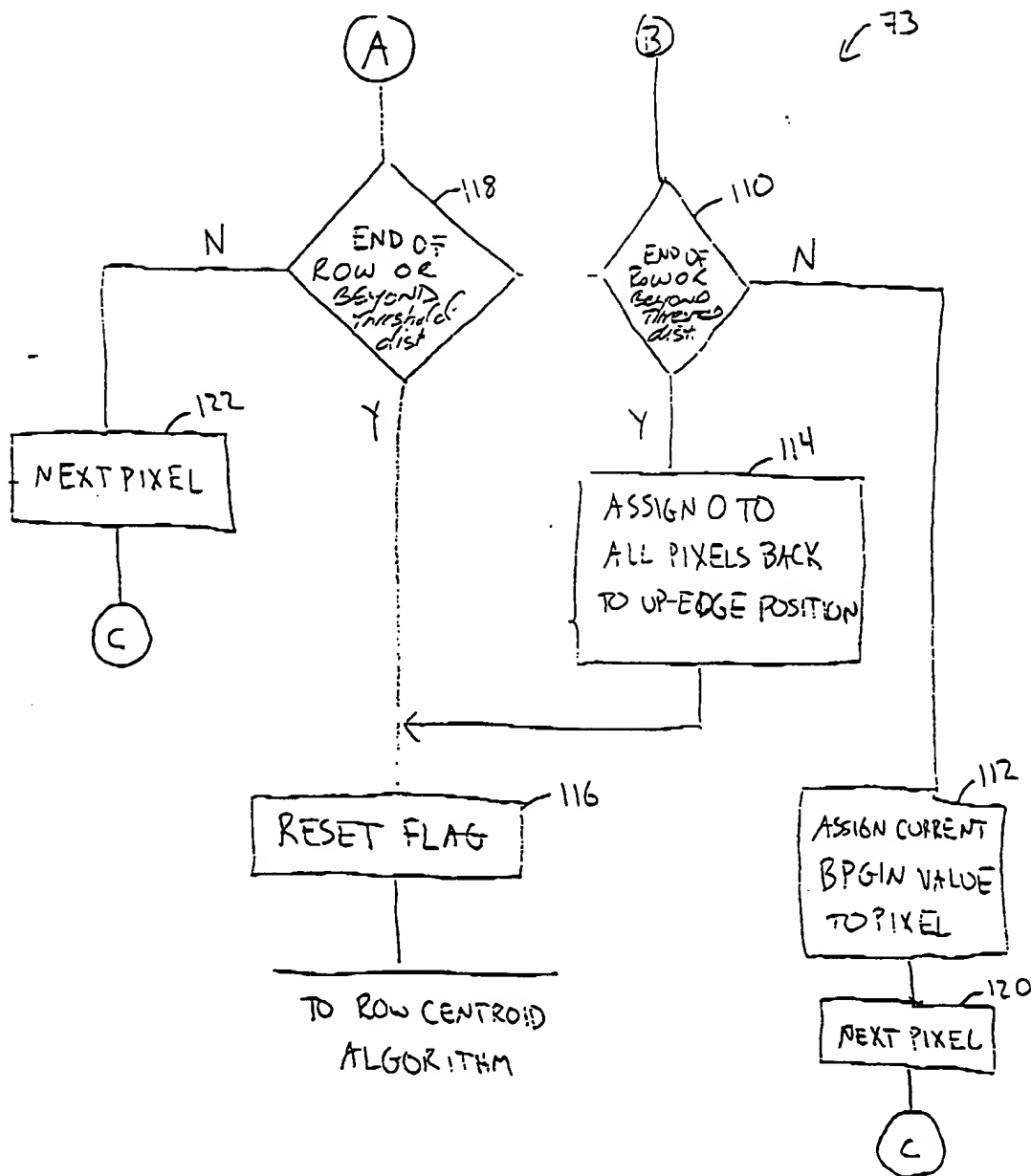


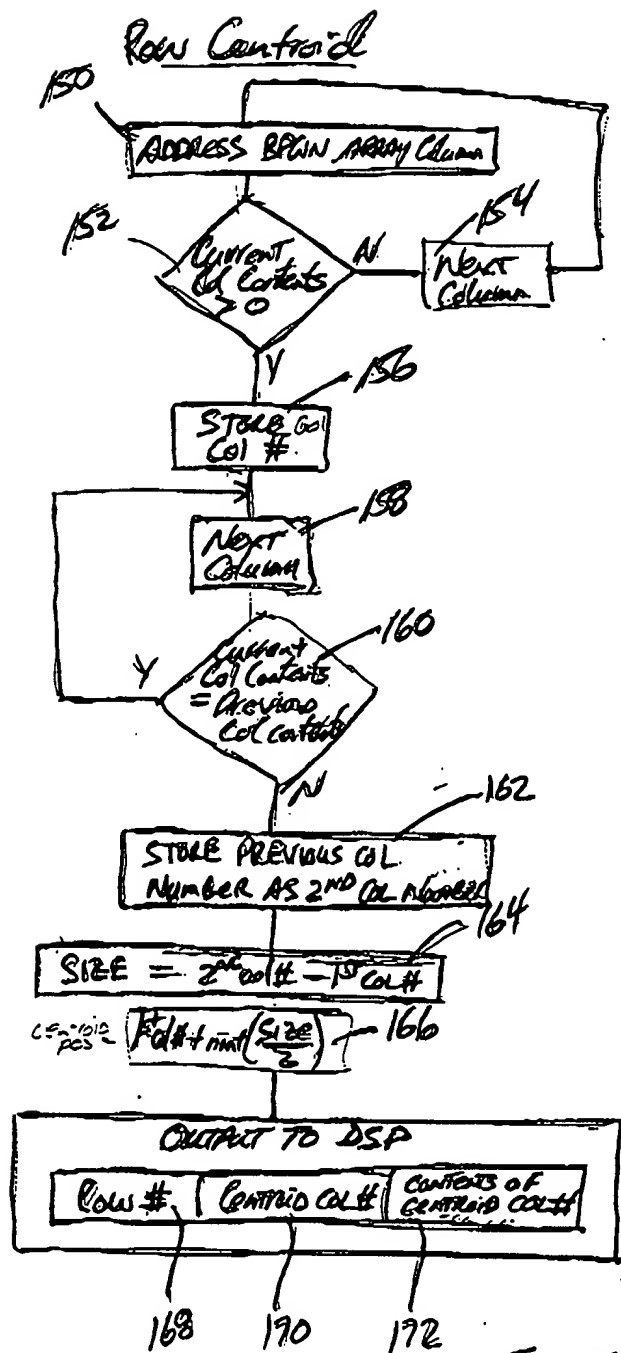
FIG. 3







FPGA



149

Fig 7

Find min
row
centroid
array

Output from Fig 7

Bright Pixel Row Centroid Array

↙ 133

Row	Col	No
12	6	1
12	15	2
13	6	3
13	16	2
13	28	5
14	5	6
14	15	2
14	28	8
15	5	9
15	16	2
15	28	11
16	5	9
16	28	11
17	5	9
17	28	11
18	6	9
18	9	12
19	9	13
20	8	13
21	10	14

Fig. 8

Bright Pixel Graping Algorithm

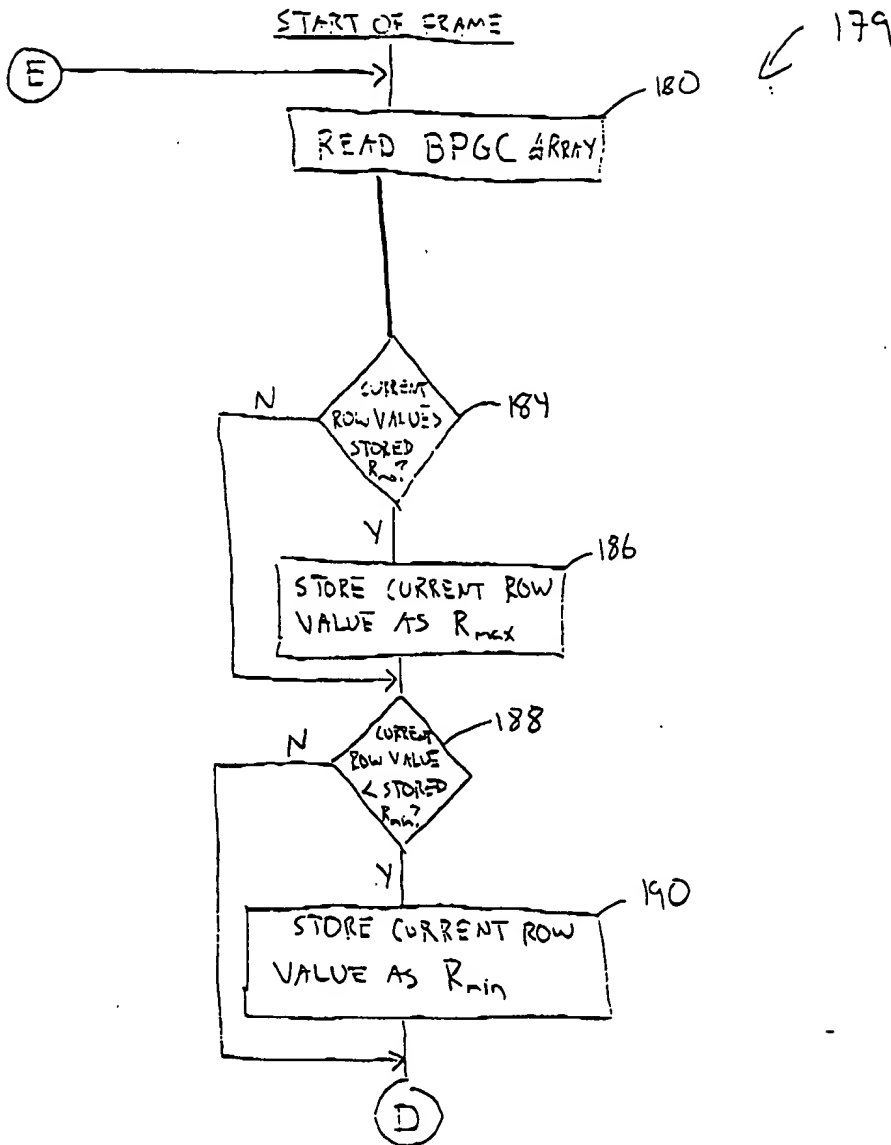


Fig 9A

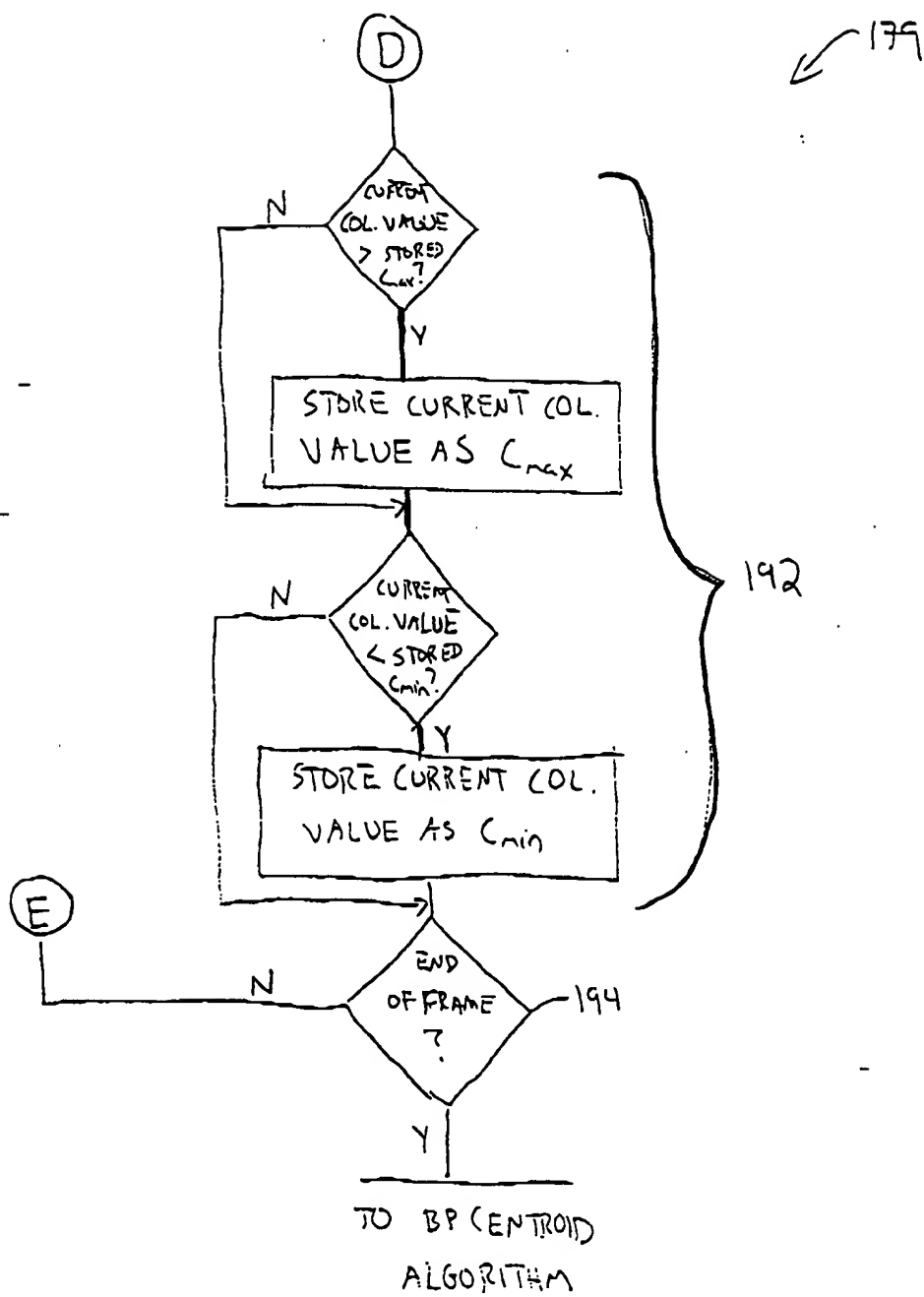


Fig. 9B.

BPG Range Array

Output From Fig 9

BPG IN	Row	Col
	MIN MAX	MIN MAX
1	12, 12	6, 6
2	12, 15	15, 16
3	13, 13	6, 6
5	13, 13	28, 28
6	14, 14	5, 5
8	14, 14	28, 28
9	15, 18	5, 6
11	15, 17	28, 28
12	18, 18	9, 9
13	19, 20	8, 9
14	21, 21	10, 10

← 300

Fig. 10

DSD

BPG Centroid Algorithm

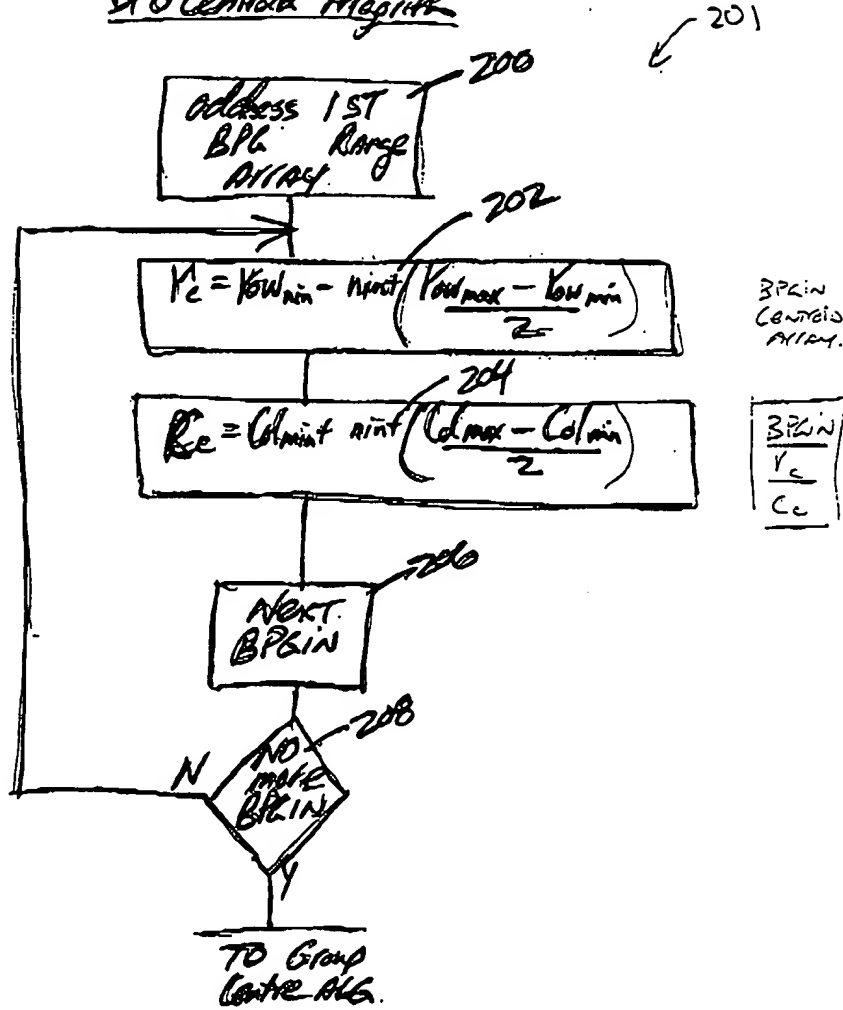


Fig 11

210 OUTPUT FROM FIG 11
 BPG CENTROID ARRAY

1 12, 6 1 ← 211
 2 13, 15 2
 3 13, 6 1

5 13, 28 5
 6 14, 5 1

8 14, 28 5
 9 16, 5 1

11 16, 28 5
 12 18, 9 1
 13 19, 8 1
 14 21, 10 1

Fig. 12

DSP

Group Centre Algorithm

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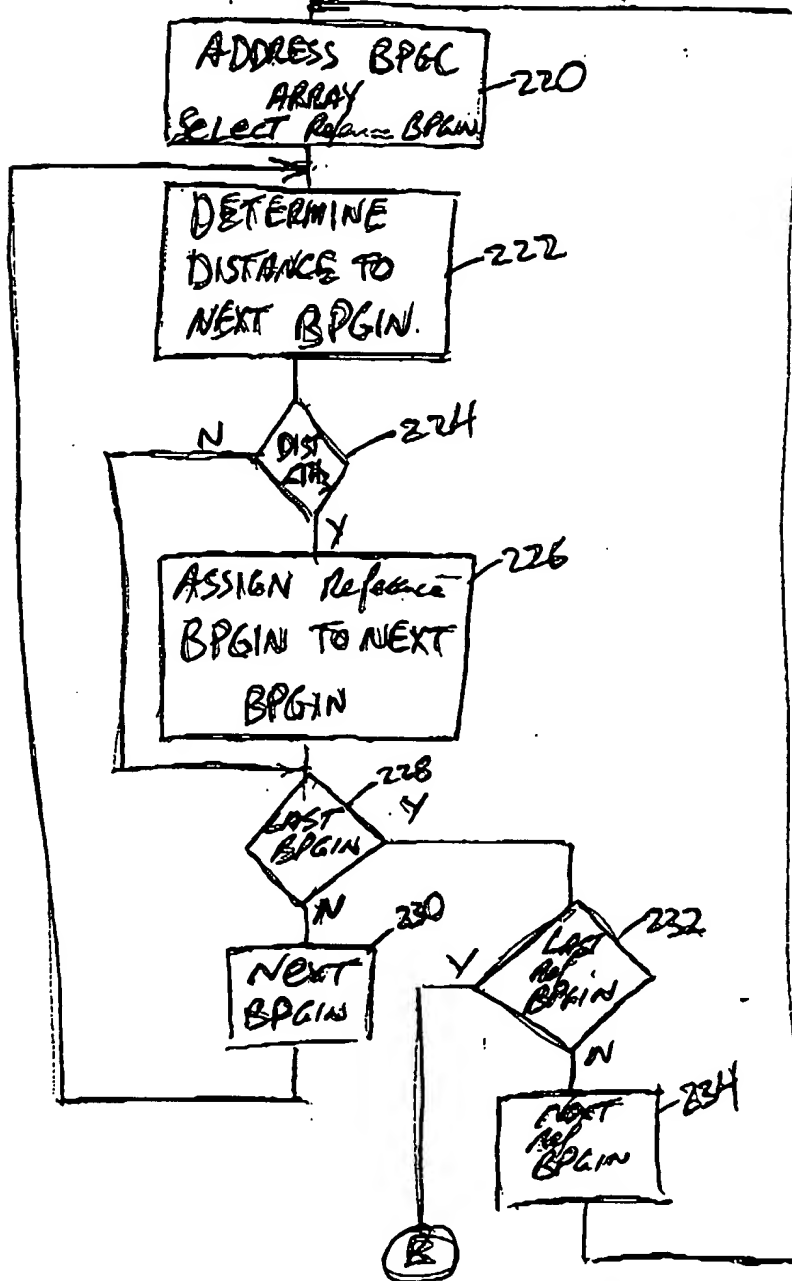


Fig 13A.

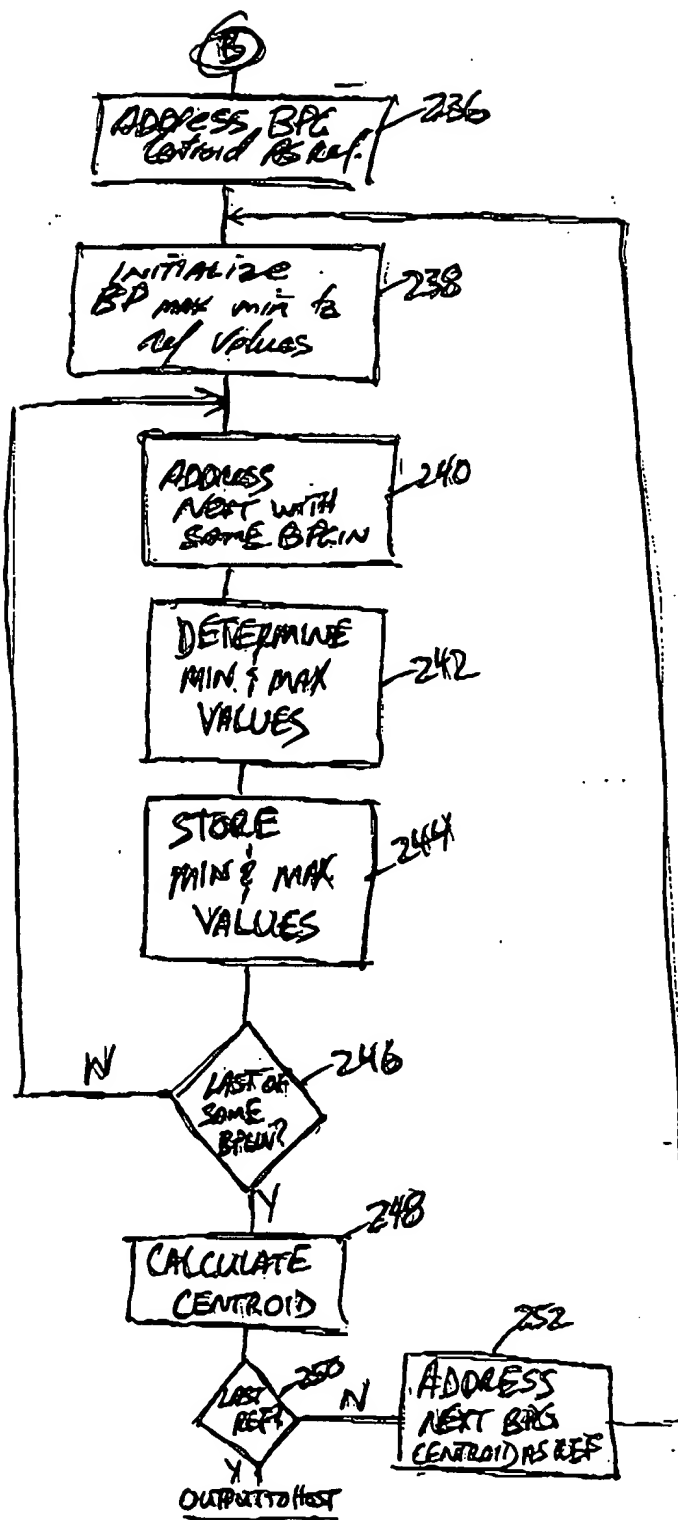


Fig. 13B

254 OUTPUT From FIG 10 WITH $\text{Th}_3 = 5$

		²⁵⁶	²⁵⁸
		Row	Column
→ 1	(12, 21, 6, 10)	16, 8	
2	(13, 13, 5, 15)	13, 15	
5	(13, 16, 28, 28)	14, 28	

Fig 14

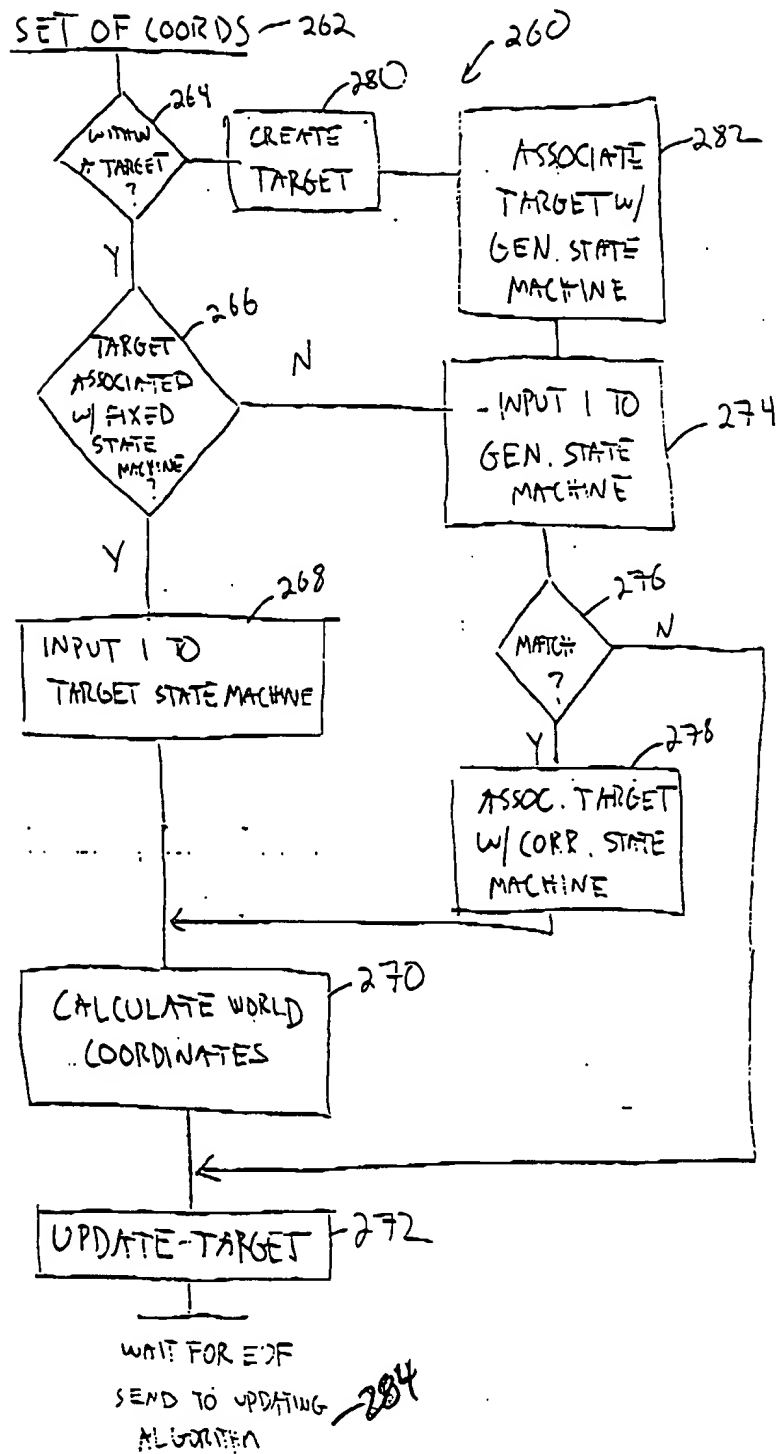


Fig 15.

Host-

Updating Algorithm

290

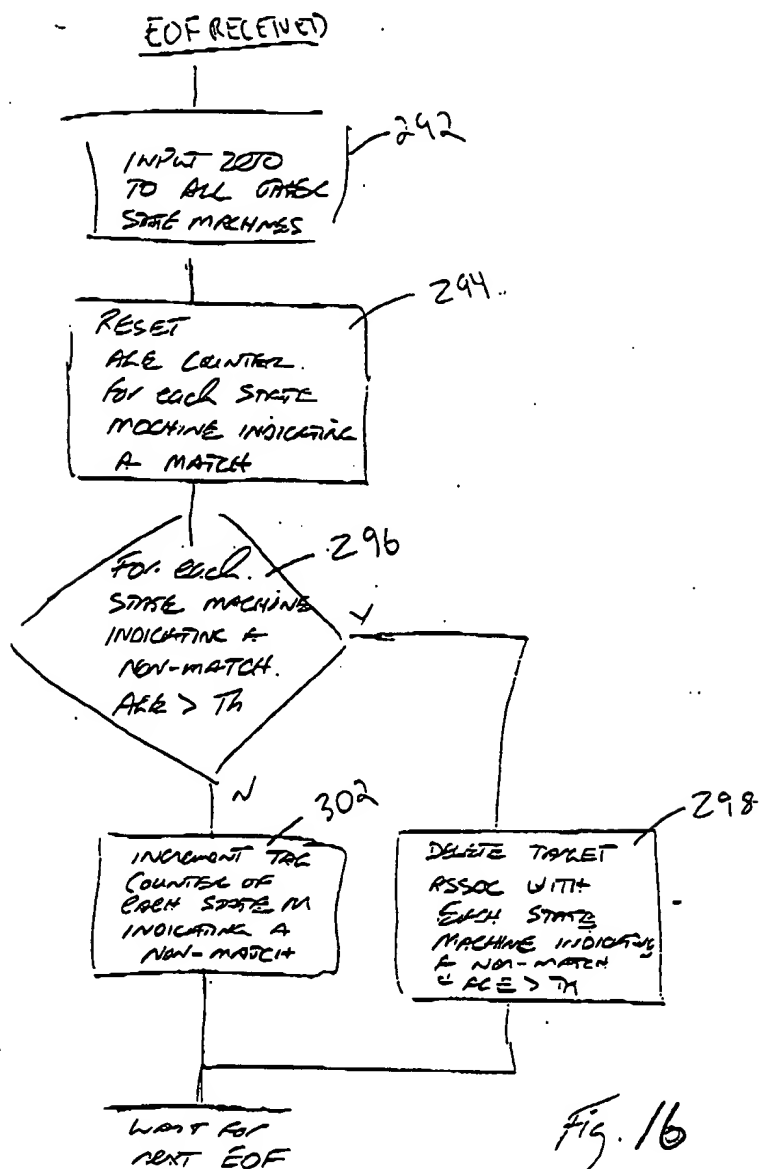


Fig. 16